REMARKS

In response to the Office Action, Applicant respectfully requests the Examiner to reconsider the above-captioned application in view of the foregoing amendments and the following comments.

Discussion of Double Patenting Rejections

In the Office Action, the Examiner rejected Claims 8 and 13-15 under 35 U.S.C. § 101 as claiming the same invention as that of claims 6, 12, 14, and 15. Applicant notes that the test for double patenting is whether a claim in the application could be literally infringed without literally infringing a corresponding claim in the patent. *See* M.P.E.P. § 804. By the present amendment, Applicant has amended independent Claim 13 to remove the recitation that the bus adapter chips provide "arbitrated access." Thus, Applicant respectfully submits that the claims are of different scope. Claim 8 has been cancelled.

Furthermore, in the Office Action, the Examiner rejected Claims 1-7, 10-12, and 16-20 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 1-7, 9-12, and 16-20 of U.S. Patent No. 6,742,069. In response, Applicant has filed a terminal disclaimer with respect to this patent, and respectfully submits that the basis of this rejection has been removed.

Applicant submits that the filing of a terminal disclaimer to obviate a rejection based on non-statutory double patenting is not an admission regarding the propriety of the rejection. *See* M.P.E.P § 804.02.

Discussion of Claim Rejections Under 35 U.S.C. § 102(e)

In the Office Action, the Examiner rejected Claims 1 and 16 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,937,174, to Weber. Applicant respectfully submits that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. *See* M.P.E.P. § 2131. Applicant respectfully submits that the cited prior art fails to teach or suggest at least one limitation from each of the above-listed claims.

Weber generally describes a hierarchical memory structure for high data bandwidth RAID applications. *See* abstract. In Weber, bus bridges 208 and 210, interconnect a processor bus 252 to buses 258 and 260. In the Office Action, the Examiner took the position that the bus bridges 206 and 208 correspond to the claimed bus adapter chips. Applicant notes that Claim 1, as amended, recites: "wherein routing the I/O buses to and from bus adapter chips comprising electrically isolating the CPU from electrical disruption when one of the interface modules is removed." Such electrical isolation helps prevent system damage if a interface module is removed during operation of the device. Claim 16 recites similar types of limitations.

Applicant respectfully submits that at least this limitation is not taught or suggested by the prior art. Applicant notes that this limitation was previously recited in dependent Claim 3 (now canceled), and that no rejection was made under §§ 102 or 103 with respect to this subject matter.

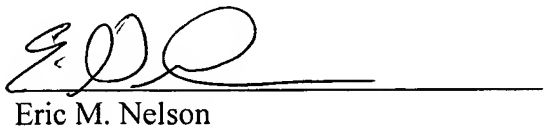
Summary

Applicant has endeavored to address all of the Examiner's concerns as expressed in the outstanding Office Action. In light of the above amendments and remarks, reconsideration and withdrawal of the outstanding rejections is respectfully requested. If the Examiner has any questions which may be answered by telephone, he is invited to call the undersigned directly.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 1/20/2006

By: 

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